FIG. 1

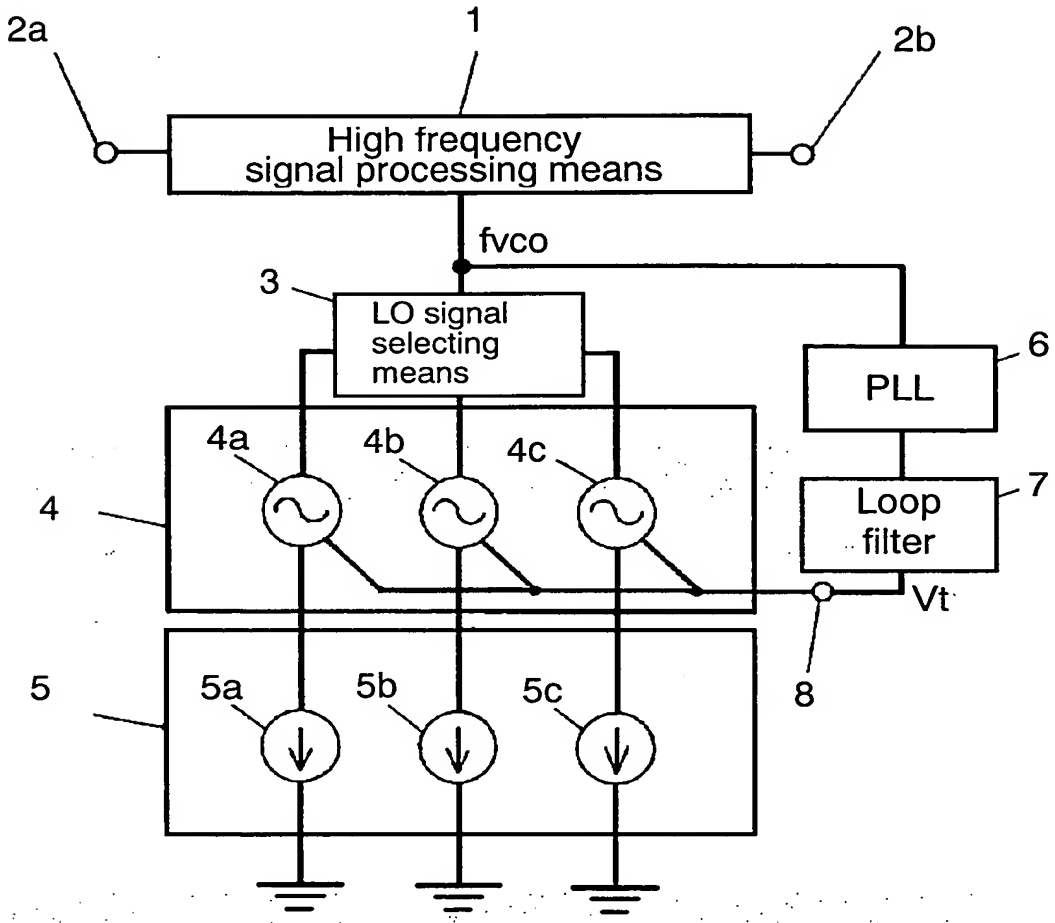

2a
1
2b
High frequency signal processing means
fvco
3
LO signal selecting means
6
PLL
4a
4b
4c
4
7
Loop filter
Vt
5
5a
5b
5c
8

FIG. 2

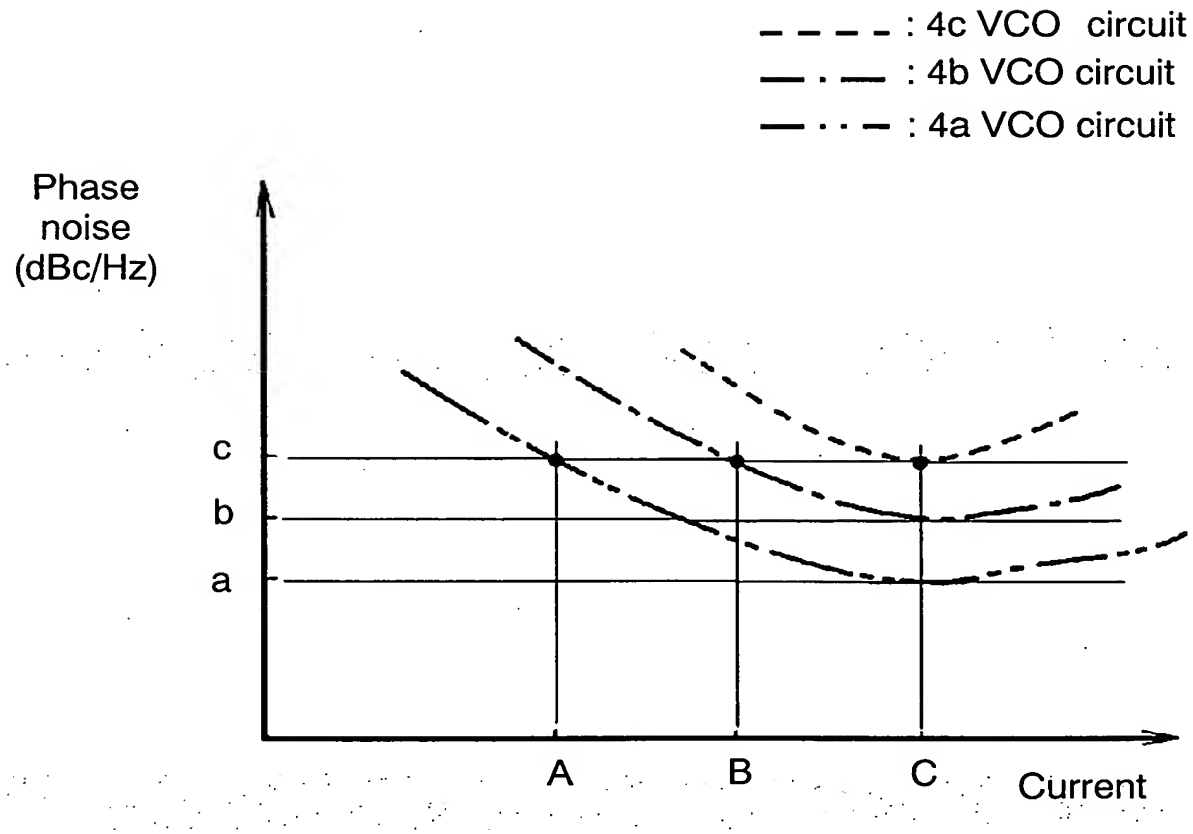

: 4c VCO circuit
: 4b VCO circuit
: 4a VCO circuit
Phase noise (dBc/Hz)
c
b
a
A
B
C
Current

FIG. 3

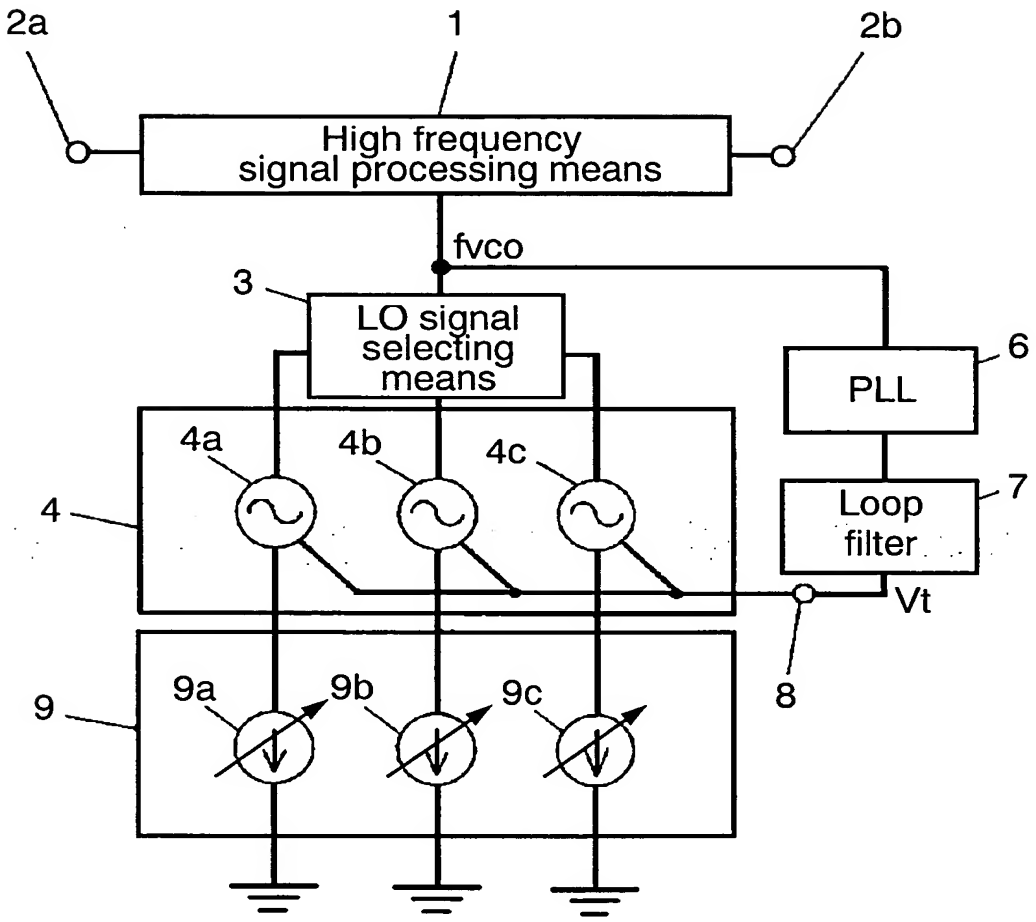

2a
1
2b
High frequency signal processing means
fvco
3
LO signal selecting means
6
PLL
4a
4b
4c
4
7
Loop filter
Vt
8
9
9a
9b
9c

FIG. 4

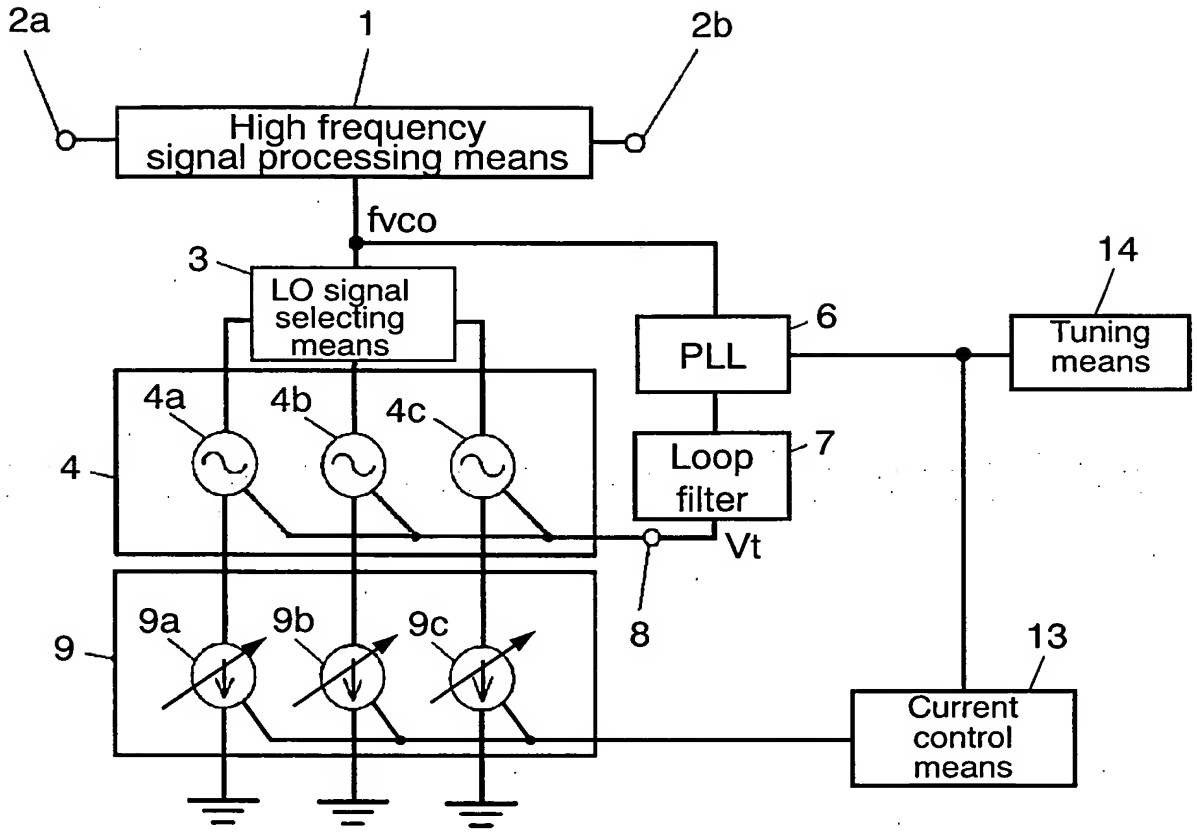

2a
1
2b
High frequency signal processing means
fvco
3
LO signal selecting means
14
PLL
6
Tuning means
4a
4b
4c
4
Loop filter
7
Vt
8
9a
9b
9c
9
13
Current control means

FIG. 5

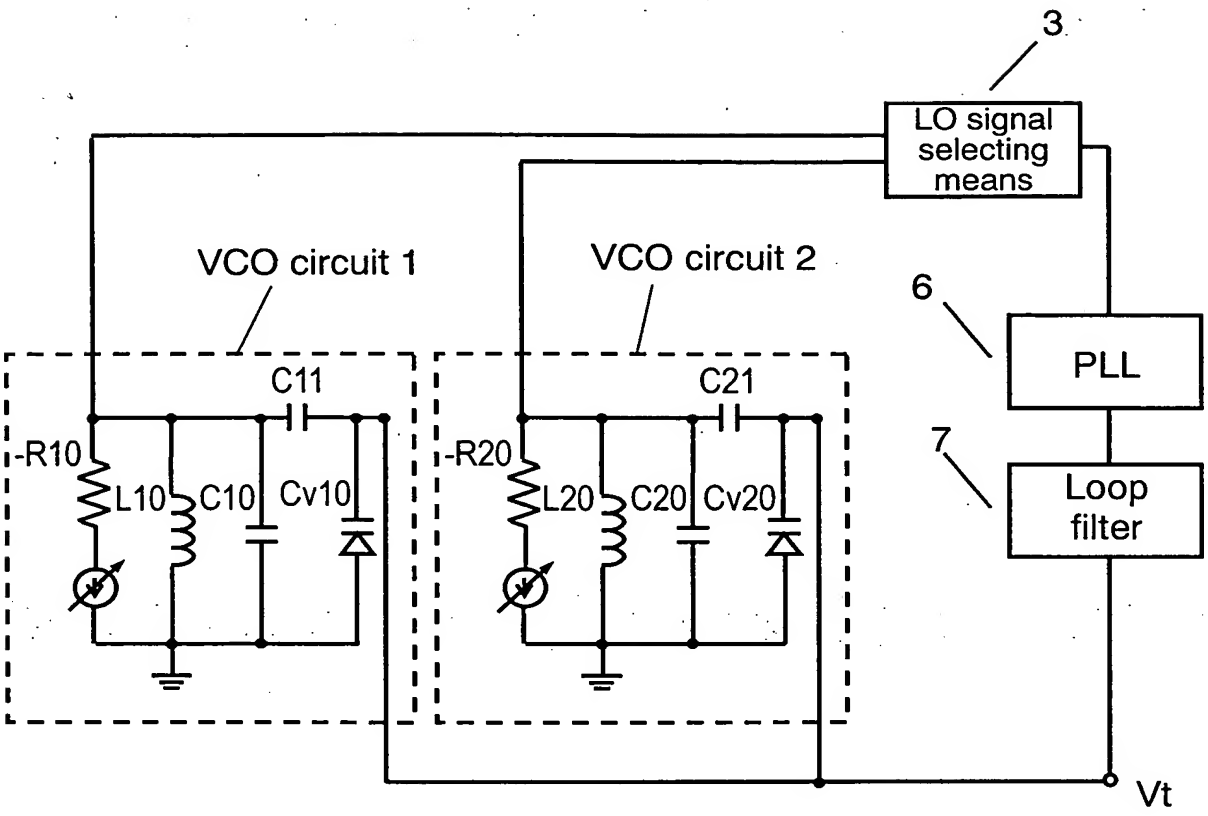

3
LO signal selecting means
VCO circuit 1
VCO circuit 2
6
PLL
7
Loop filter
C11
C21
-R10
L10
C10
Cv10
-R20
L20
C20
Cv20
Vt

FIG. 6

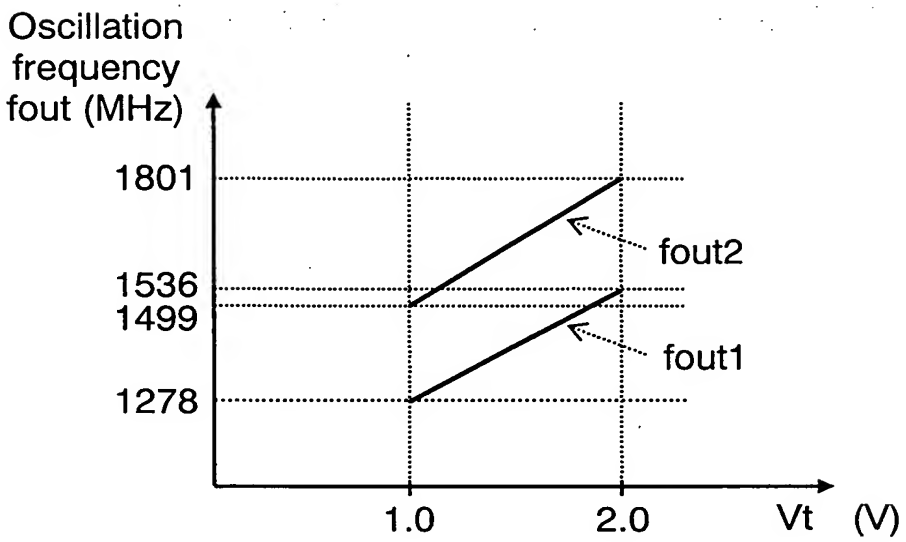

Oscillation
frequency
fout (MHz)
1801
1536
1499
1278
fout2
fout1
1.0
2.0
Vt (V)

FIG. 7

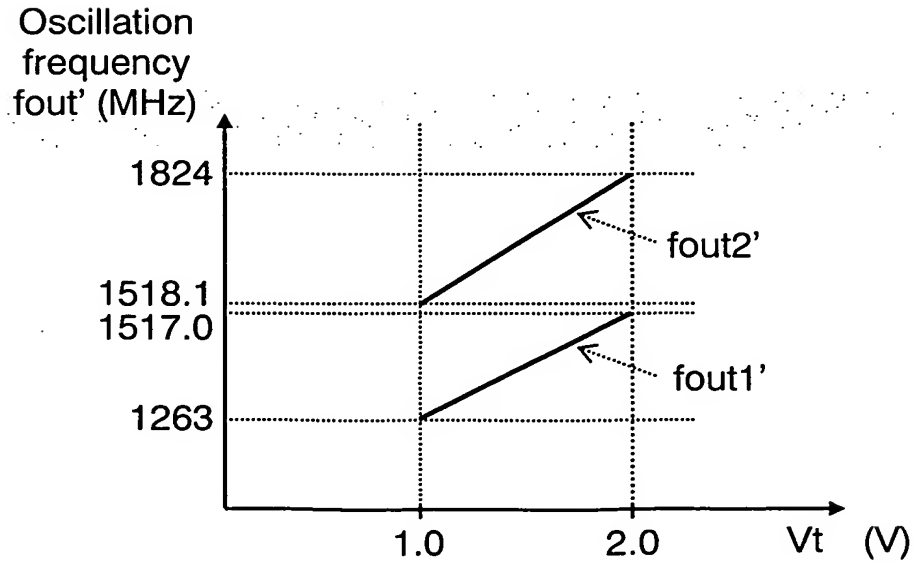

Oscillation
frequency
fout' (MHz)
1824
1518.1
1517.0
1263
fout2'
fout1'
1.0
2.0
Vt (V)

FIG. 8

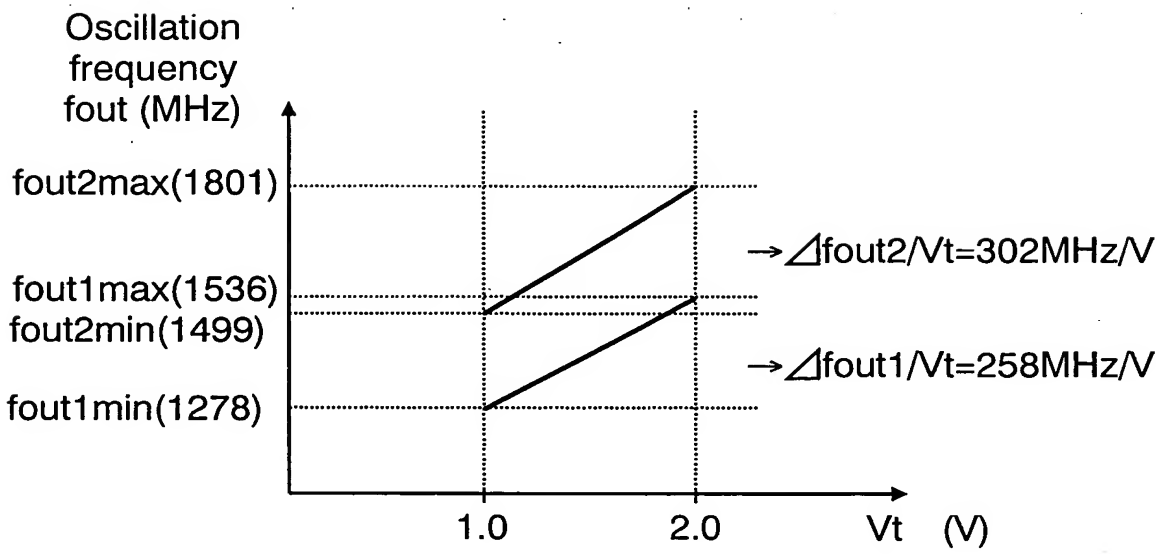

Oscillation
frequency
fout (MHz)
fout2max(1801)
fout1max(1536)
fout2min(1499)
fout1min(1278)
→⊿fout2/Vt=302MHz/V
→⊿fout1/Vt=258MHz/V
1.0
2.0
Vt (V)

FIG. 9

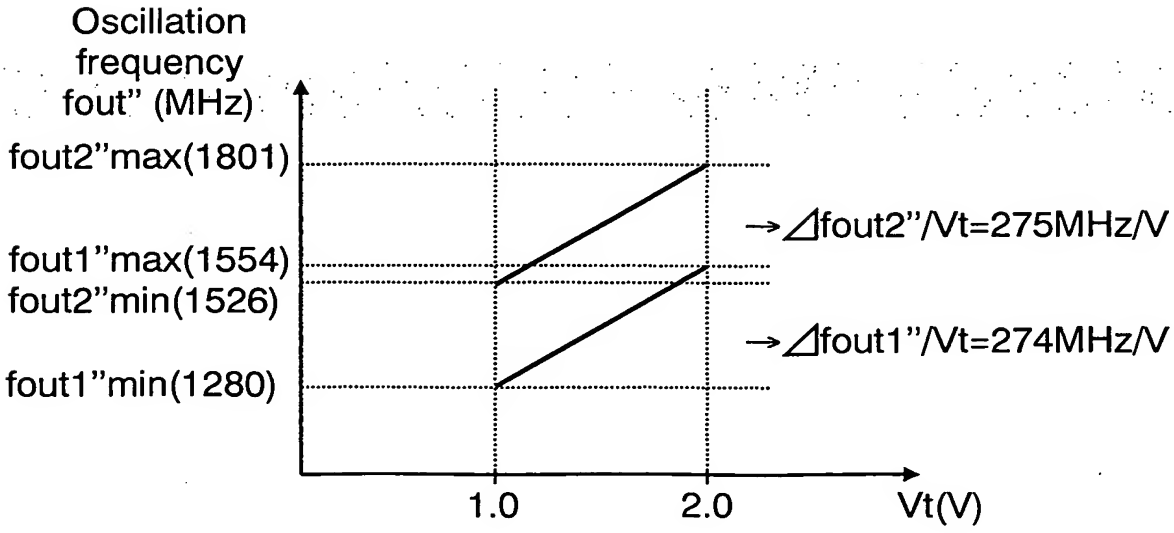

Oscillation
frequency
fout" (MHz)
fout2"max(1801)
fout1"max(1554)
fout2"min(1526)
fout1"min(1280)
→⊿fout2"/Vt=275MHz/V
→⊿fout1"/Vt=274MHz/V
1.0
2.0
Vt(V)

FIG. 10

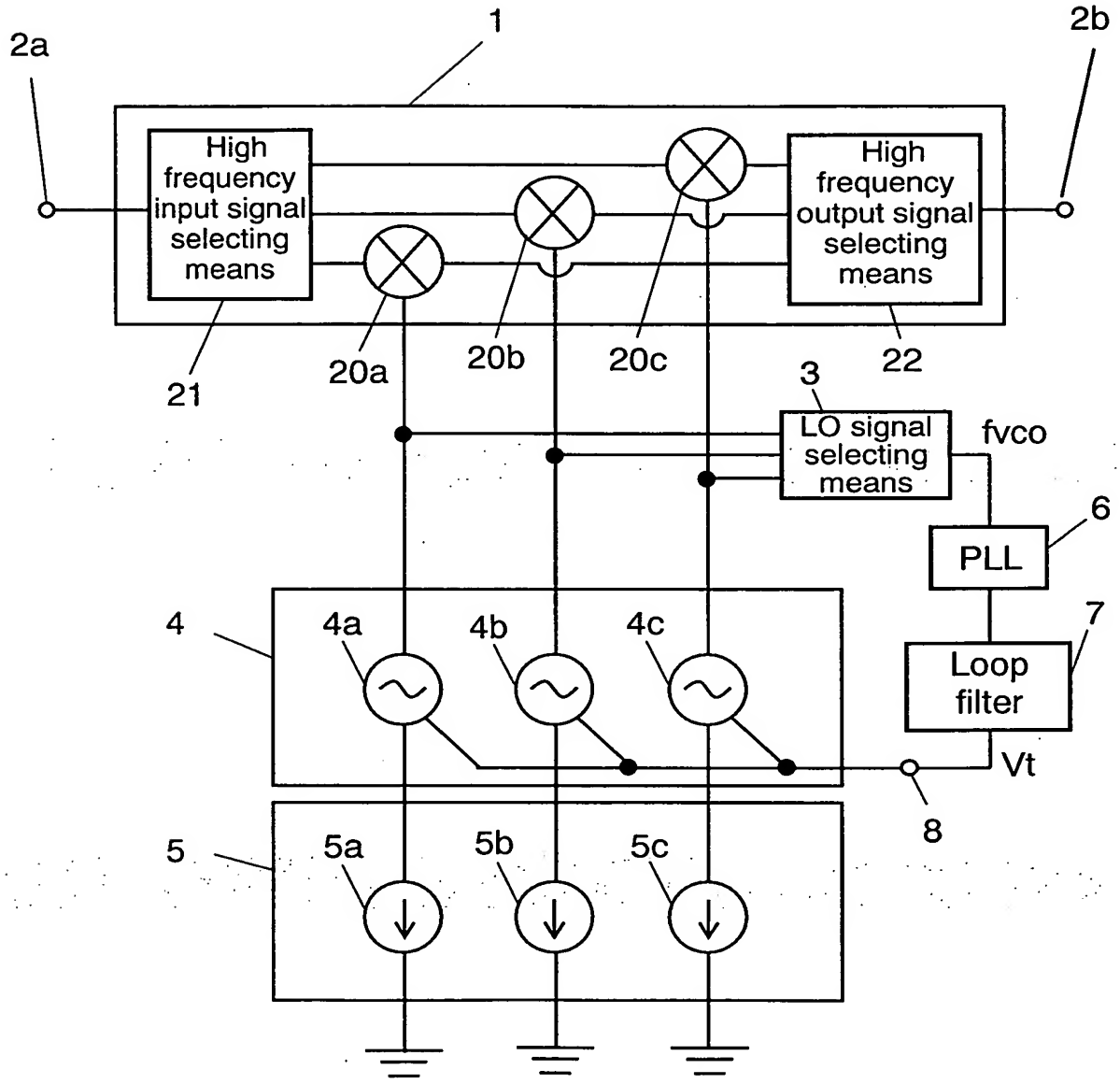

1
2a
2b
High frequency input signal selecting means
High frequency output signal selecting means
21
20a
20b
20c
22
3
LO signal selecting means
fvco
6
PLL
7
Loop filter
Vt
8
4
4a
4b
4c
5
5a
5b
5c

FIG. 11

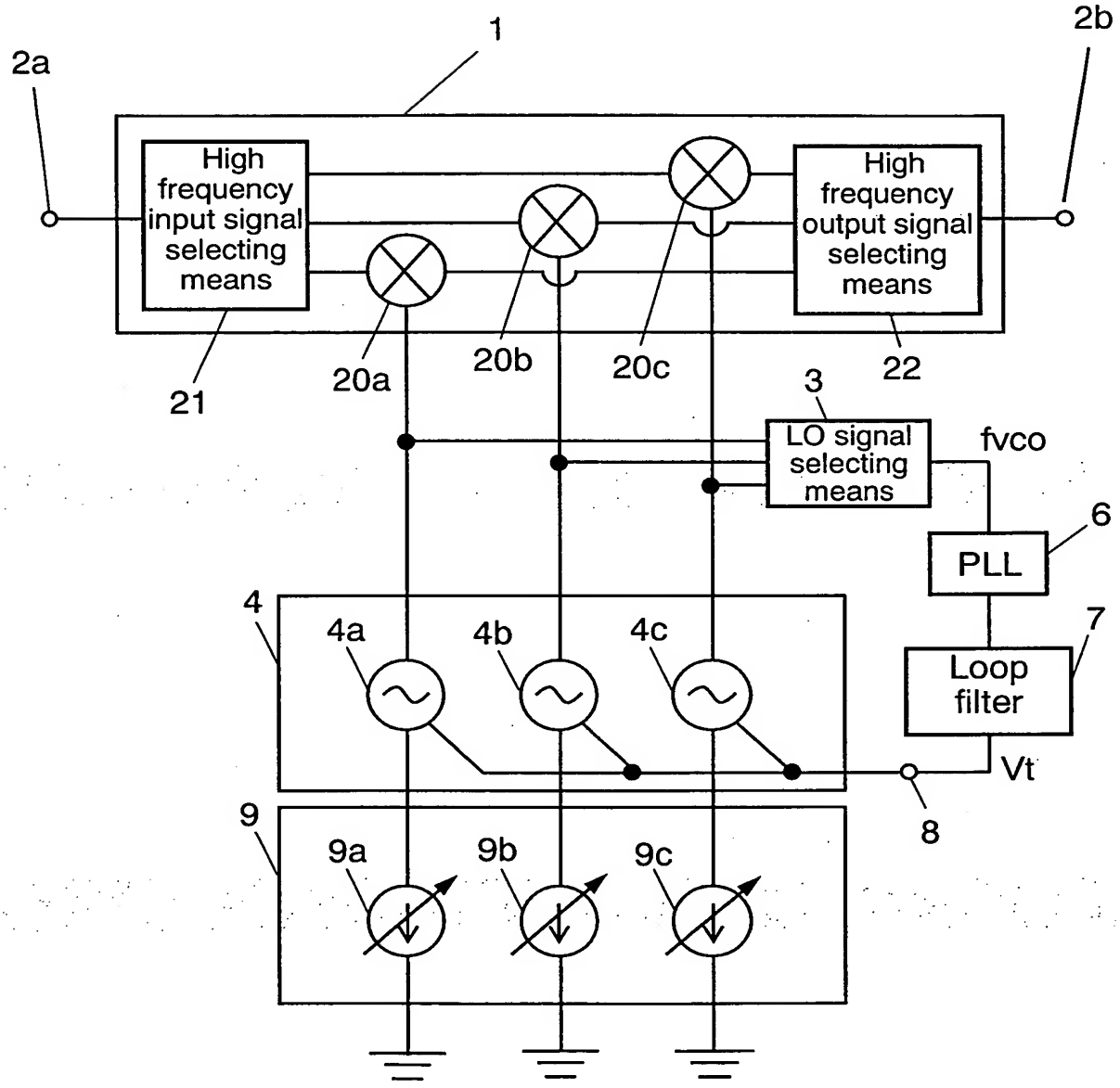

1
2a
2b
High frequency input signal selecting means
High frequency output signal selecting means
21
20a
20b
20c
22
3
LO signal selecting means
fvco
6
PLL
4
4a
4b
4c
7
Loop filter
Vt
8
9
9a
9b
9c

FIG. 12

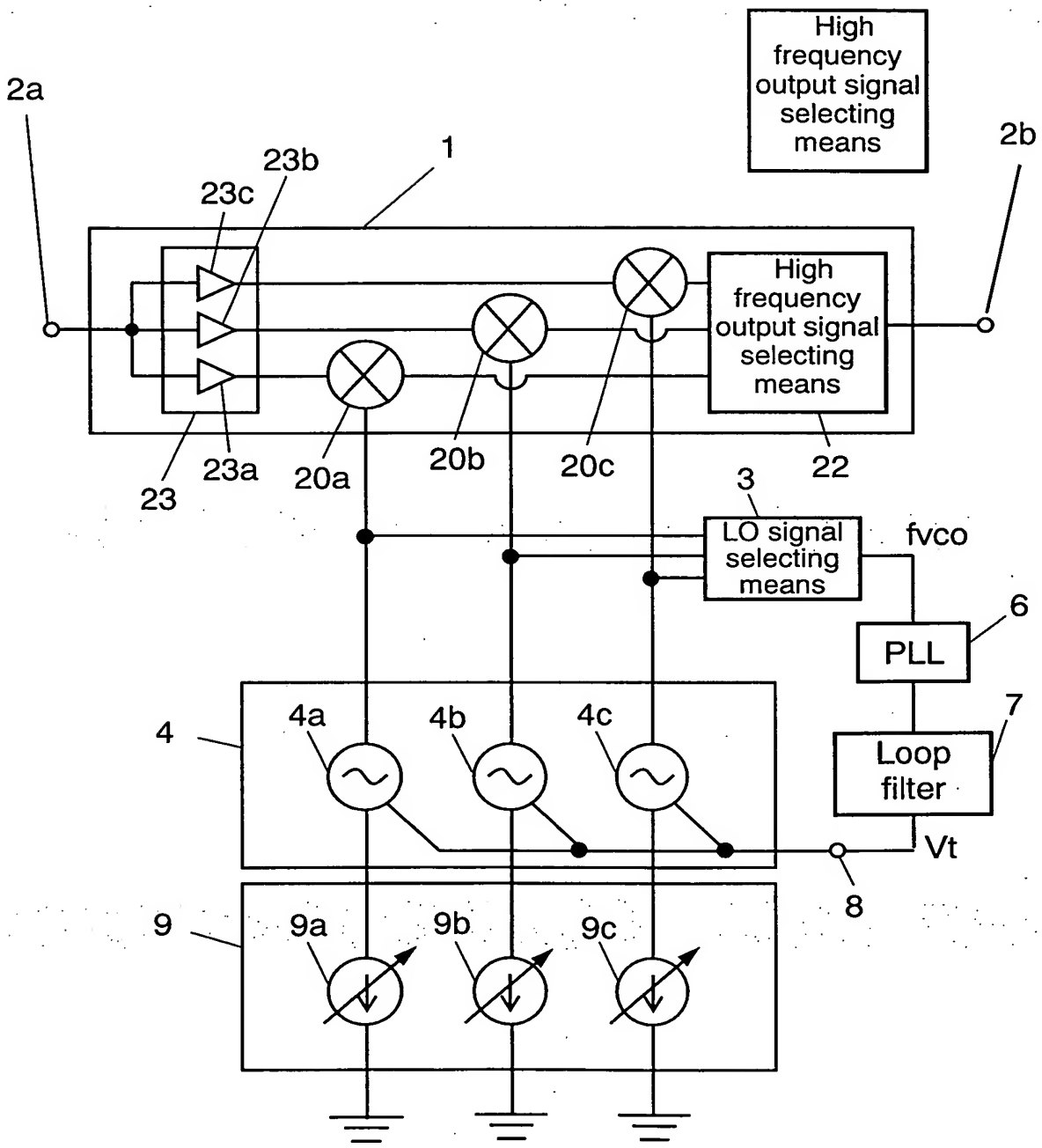

High frequency output signal selecting means
2a
2b
1
23b
23c
23
23a
20a
20b
20c
22
High frequency output signal selecting means
3
LO signal selecting means
fvco
6
PLL
7
Loop filter
Vt
8
4
4a
4b
4c
9
9a
9b
9c

FIG. 13

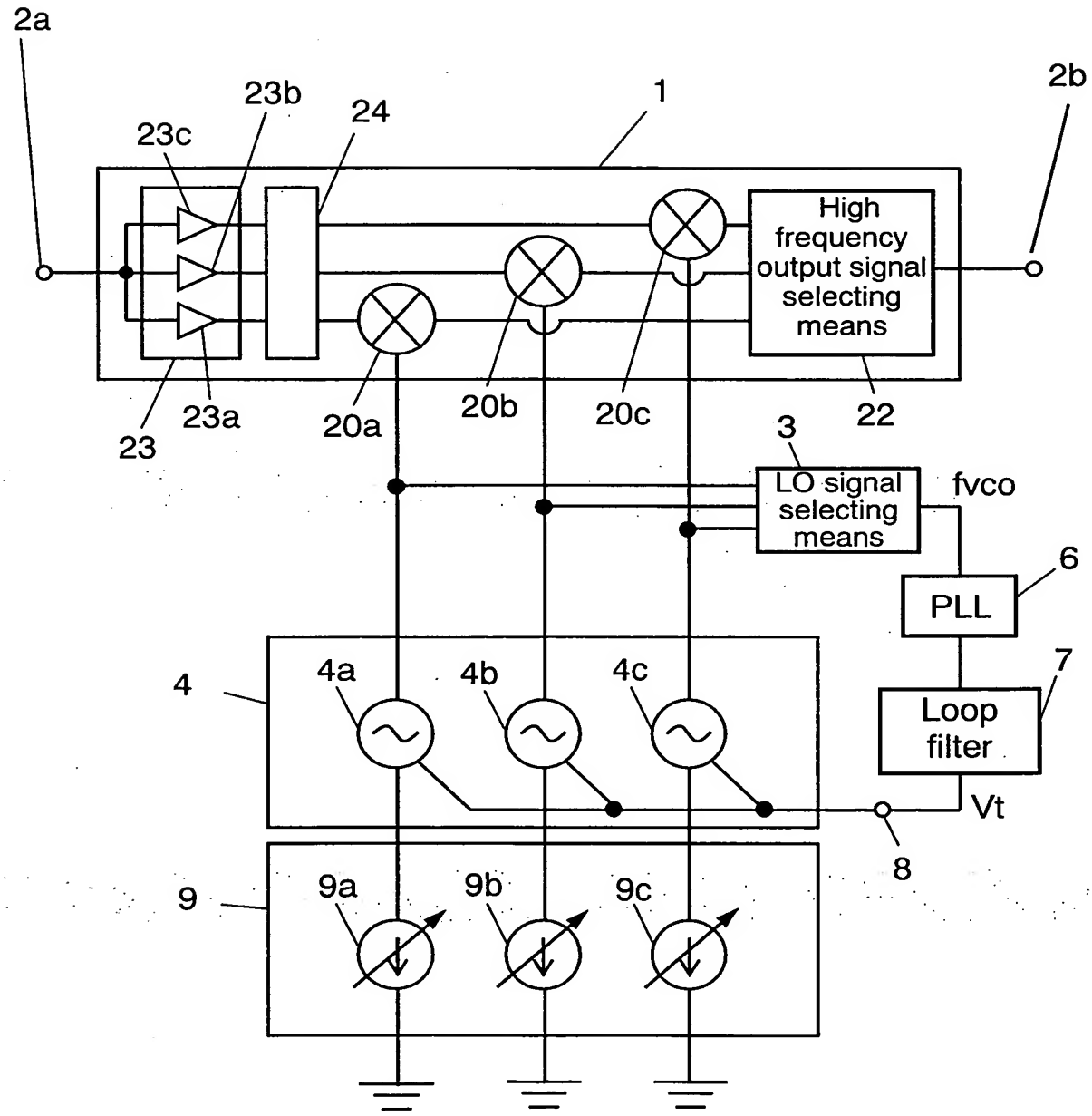

2a
23b
24
1
2b
23c
High frequency output signal selecting means
23
23a
20a
20b
20c
22
3
LO signal selecting means
fvco
6
PLL
4
4a
4b
4c
7
Loop filter
Vt
8
9
9a
9b
9c

FIG. 14

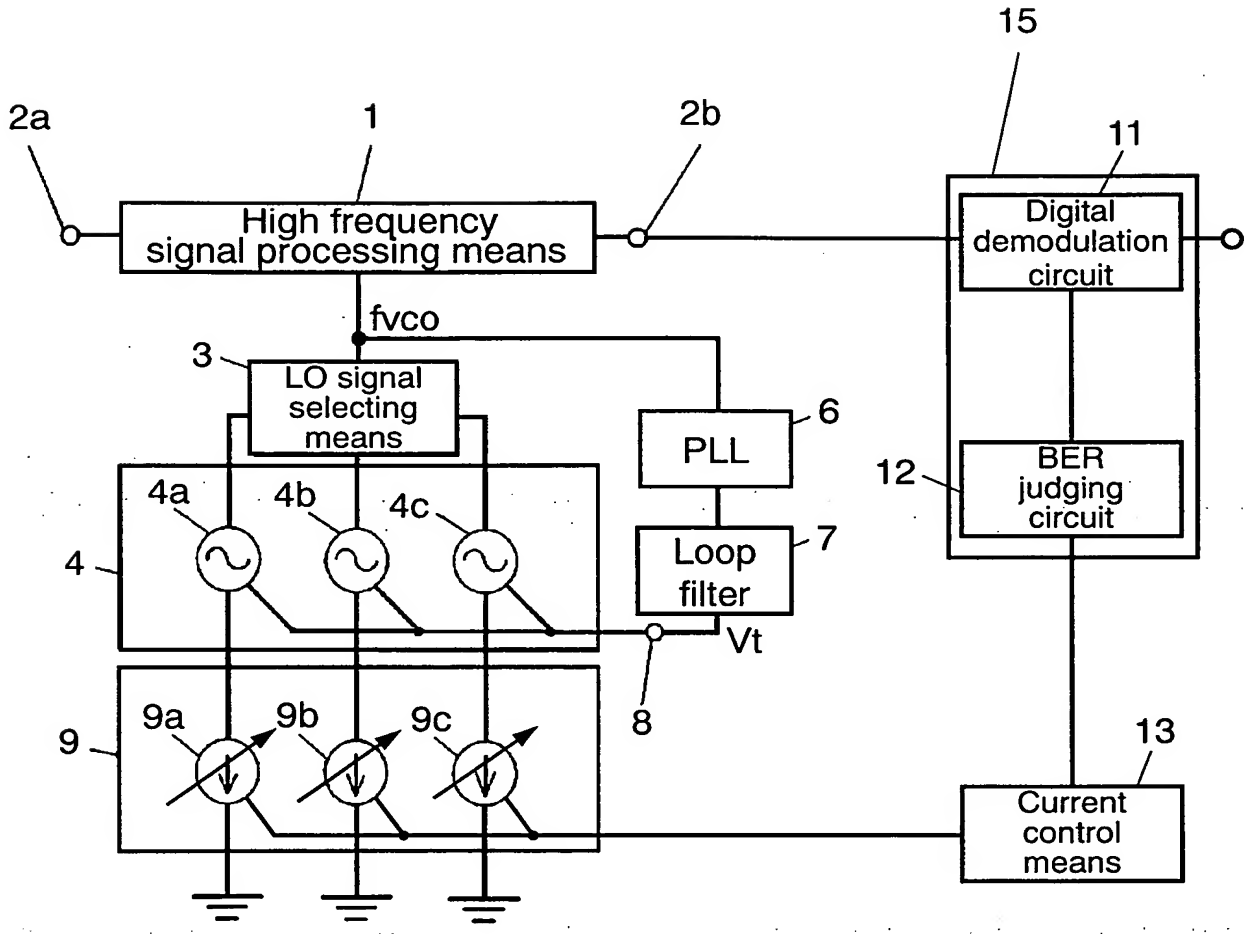

15
2a
1
2b
11
High frequency signal processing means
Digital demodulation circuit
fvco
3
LO signal selecting means
PLL
6
BER judging circuit
12
4a
4b
4c
4
Loop filter
7
Vt
8
9a
9b
9c
9
13
Current control means

FIG. 15

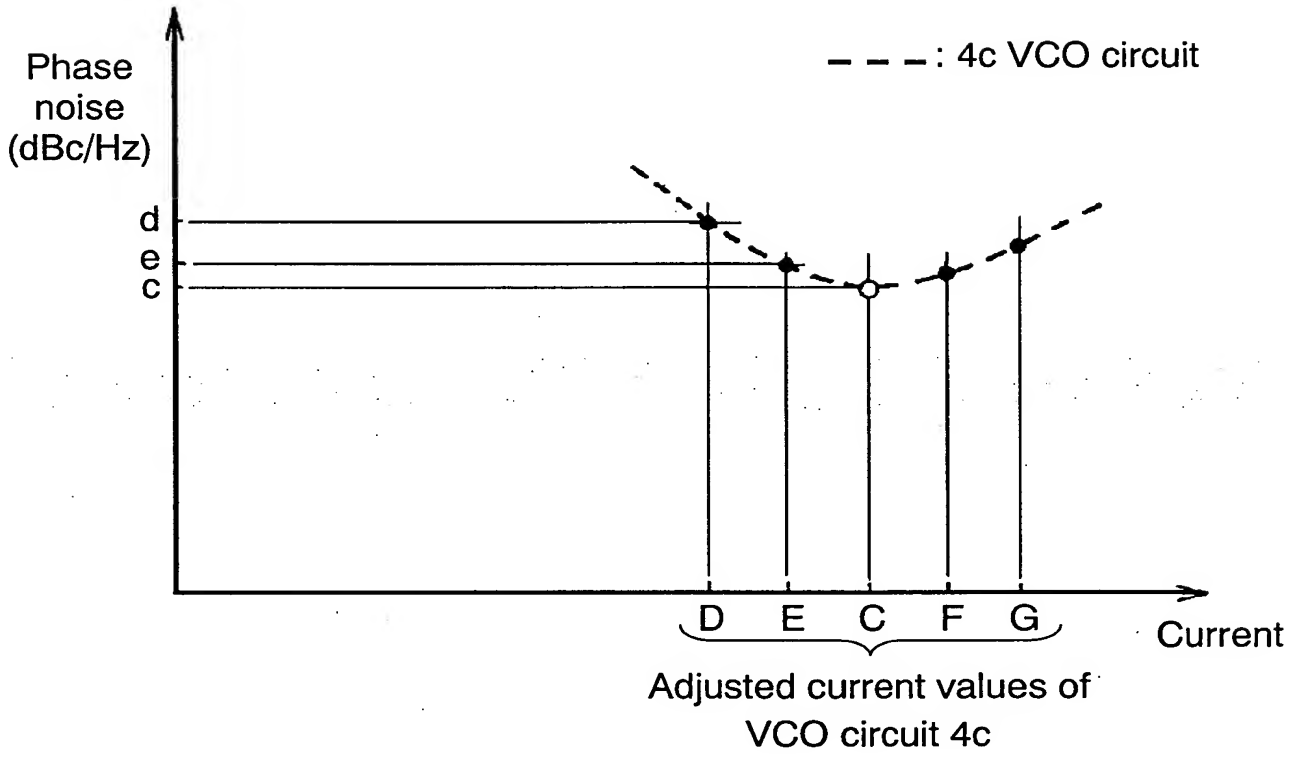

Phase noise (dBc/Hz)
– – –: 4c VCO circuit
d
e
c
D
E
C
F
G
Current
Adjusted current values of VCO circuit 4c

FIG. 16

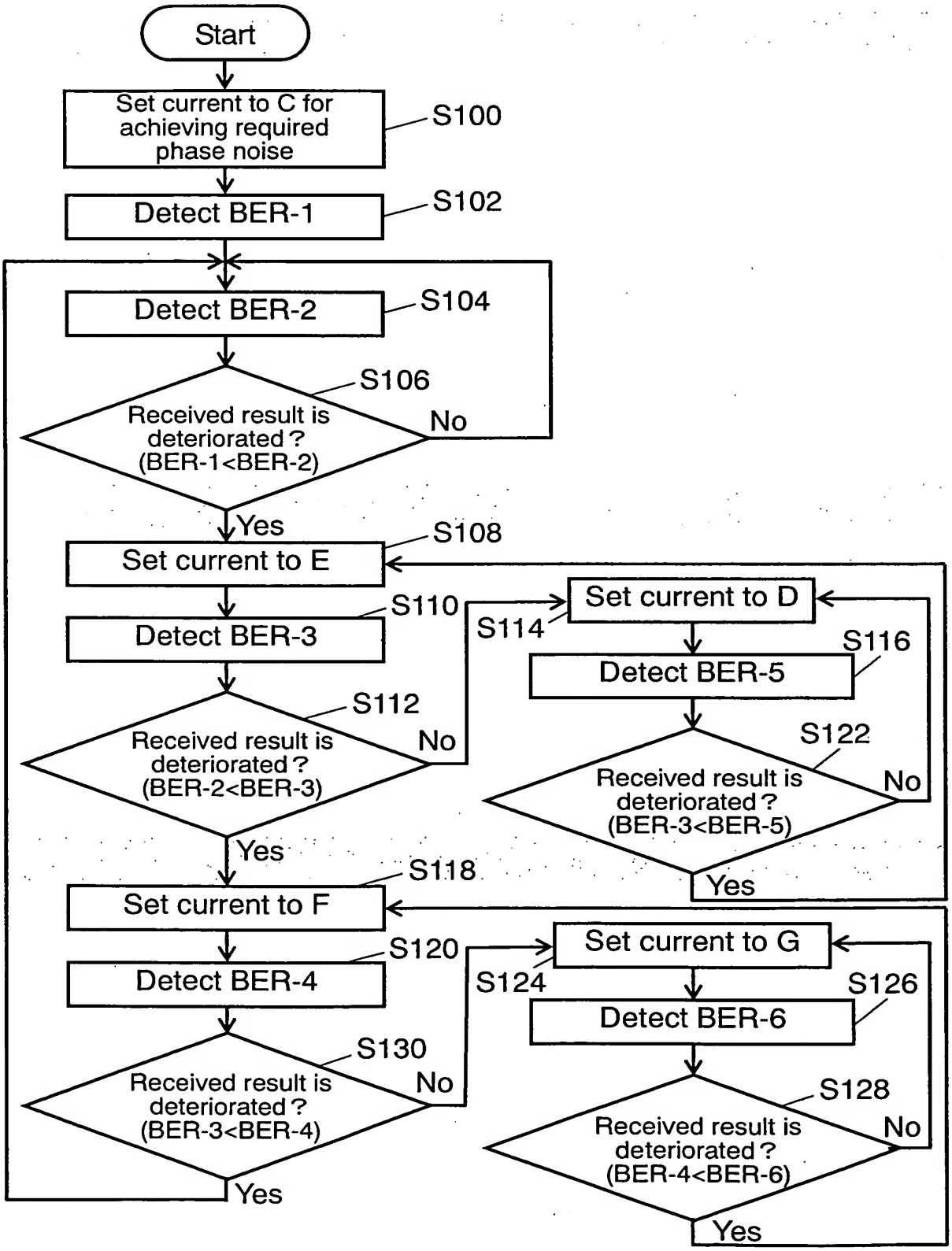

Start
Set current to C for achieving required phase noise
S100
Detect BER-1
S102
Detect BER-2
S104
Received result is deteriorated? (BER-1<BER-2)
S106
No
Yes
Set current to E
S108
Detect BER-3
S110
Received result is deteriorated? (BER-2<BER-3)
S112
No
Yes
Set current to D
S114
Detect BER-5
S116
Received result is deteriorated? (BER-3<BER-5)
S122
No
Yes
Set current to F
S118
Detect BER-4
S120
Received result is deteriorated? (BER-3<BER-4)
S130
No
Yes
Set current to G
S124
Detect BER-6
S126
Received result is deteriorated? (BER-4<BER-6)
S128
No
Yes

FIG. 17

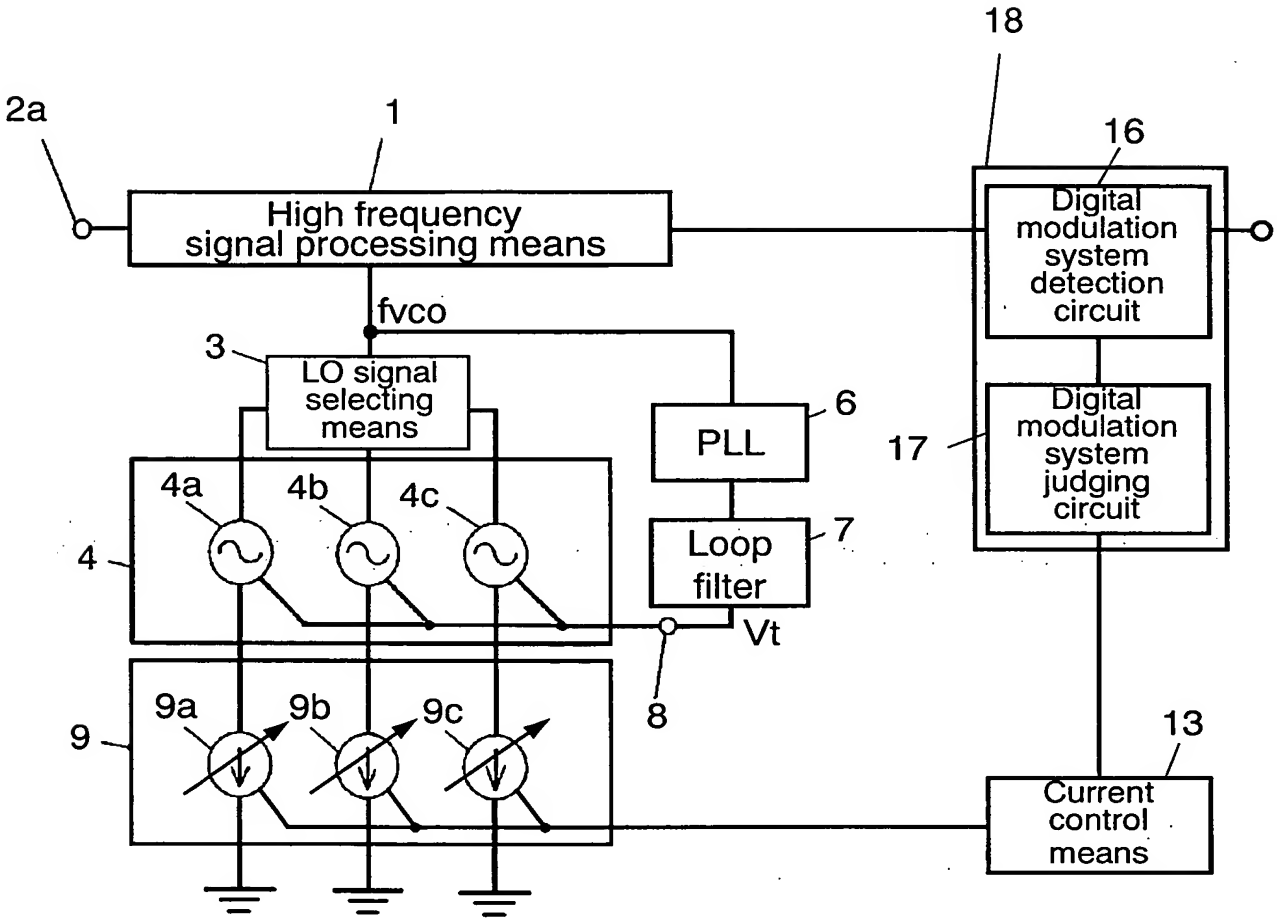

18
2a
1
16
High frequency signal processing means
Digital modulation system detection circuit
fvco
3
LO signal selecting means
6
PLL
17
Digital modulation system judging circuit
4a
4b
4c
4
Loop filter
7
Vt
8
9a
9b
9c
9
13
Current control means

FIG. 18

Digital modulation system (required CNR of receiver)	Modulation system (1) (required CNR=large)		Modulation system (2) (required CNR=middle)		Modulation system (3) (required CNR=small)
Phase noise and current amount of VCO	Phase noise=c	<	Phase noise=e	<	Phase noise=d
	Current amount=C	>	Current amount=E	>	Current amount=D

FIG. 19

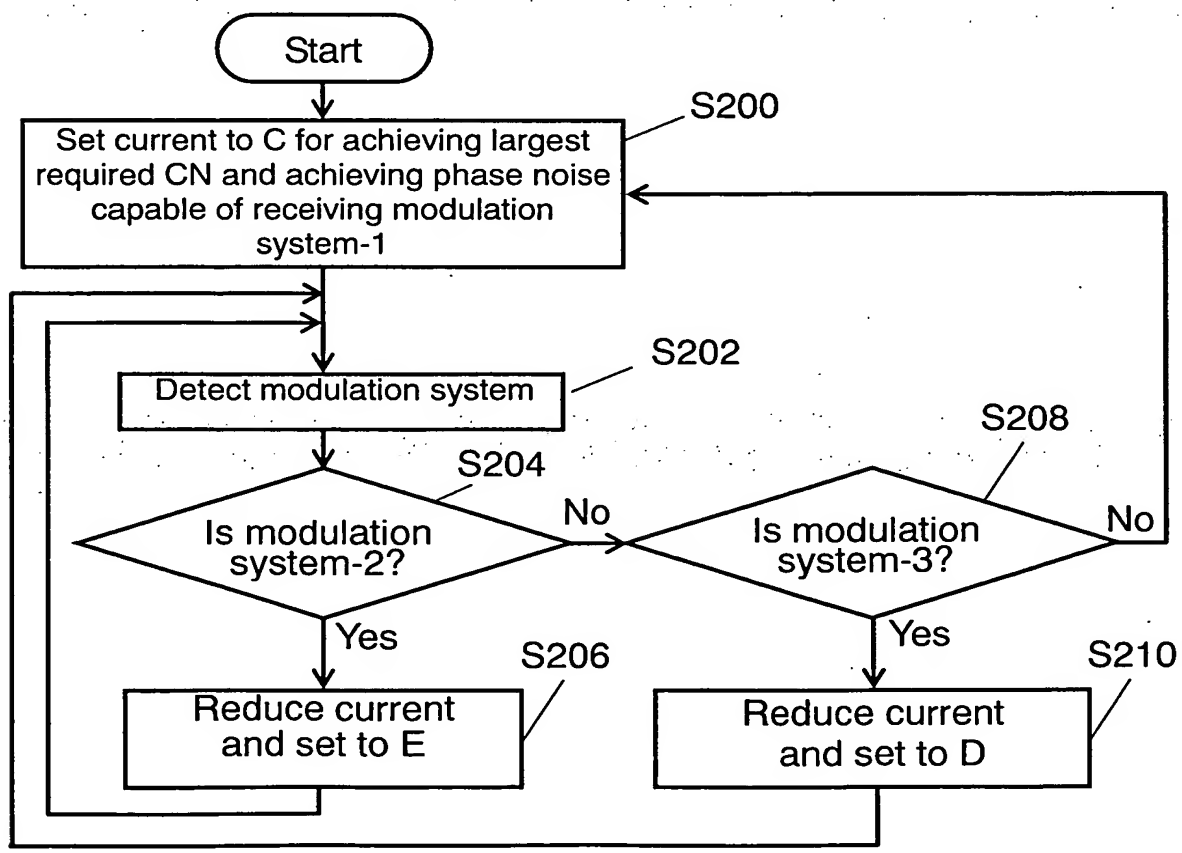


FIG. 20

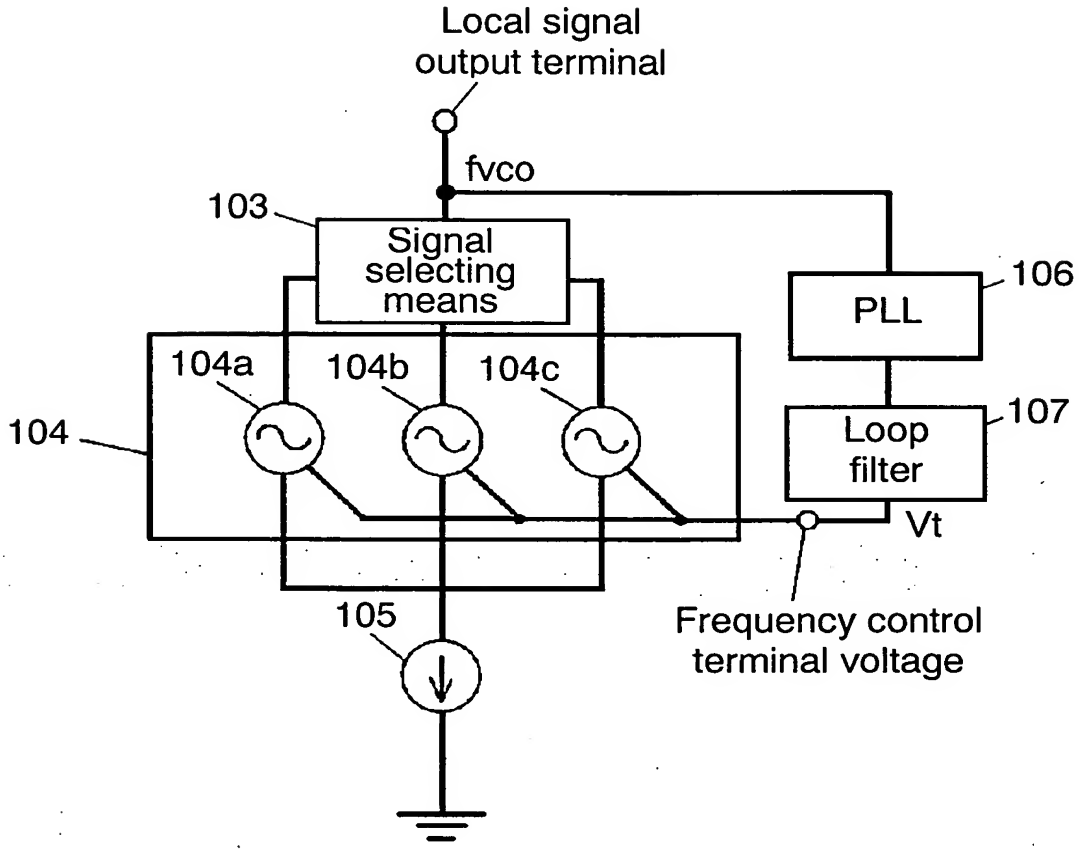

Local signal
output terminal
fvco
103
Signal
selecting
means
106
PLL
104a
104b
104c
104
107
Loop
filter
Vt
105
Frequency control
terminal voltage

FIG. 21

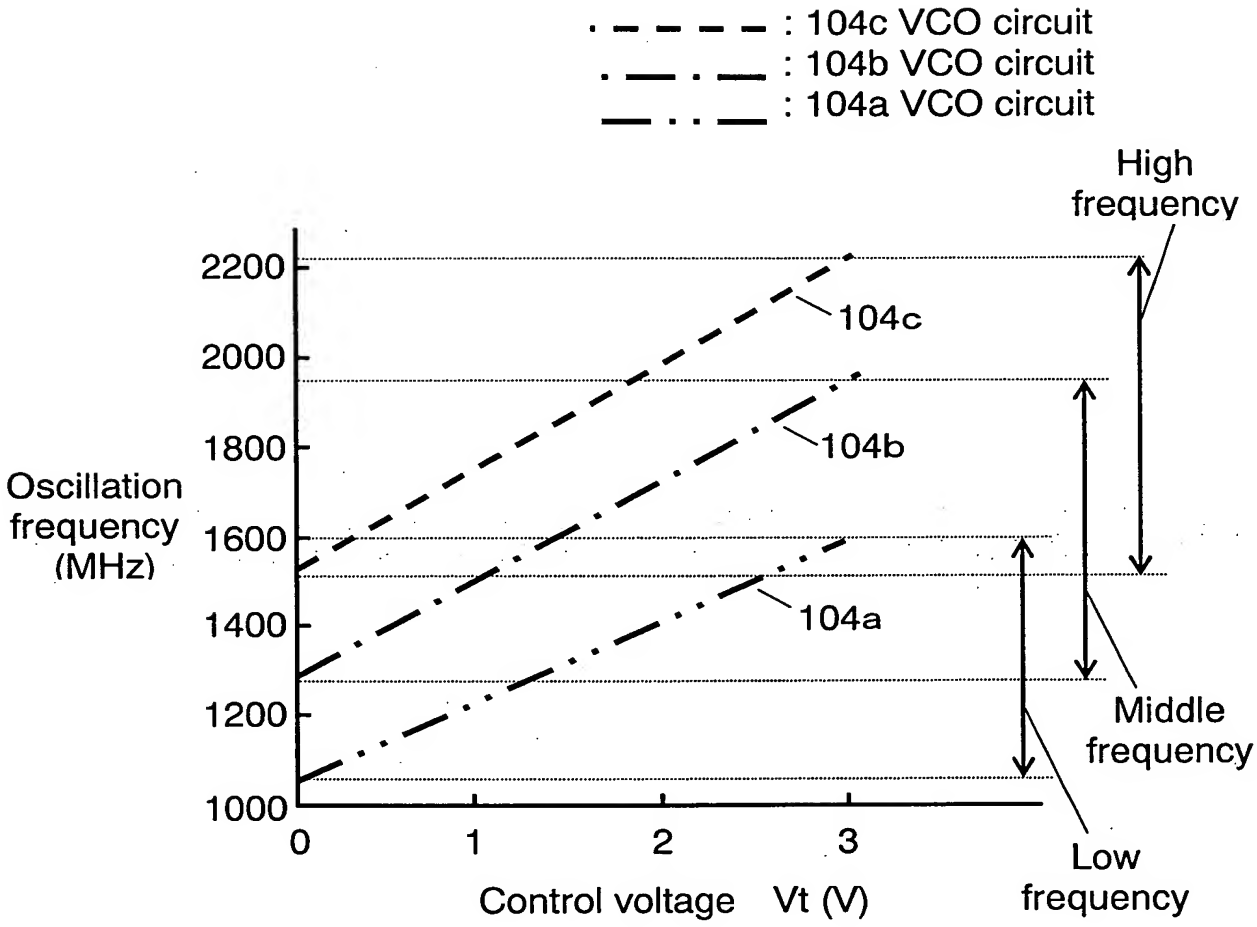
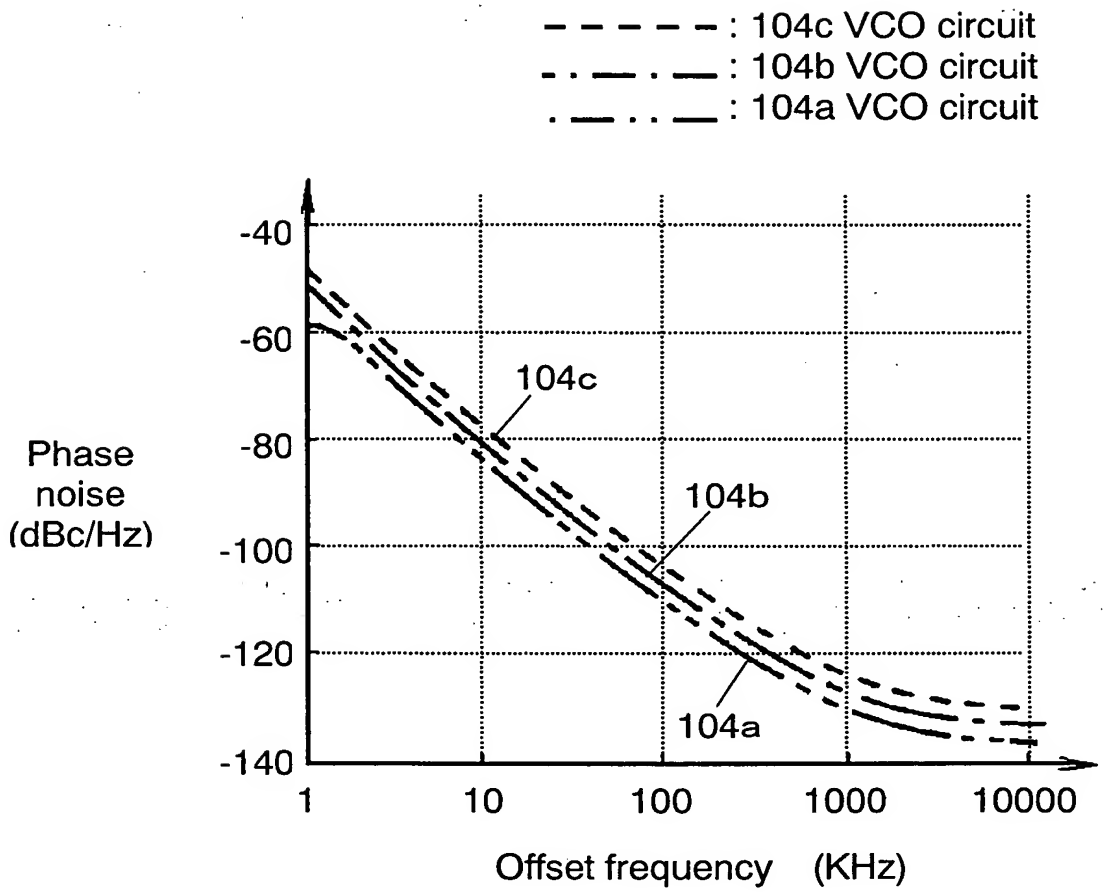

: 104c VCO circuit
: 104b VCO circuit
: 104a VCO circuit
High frequency
Middle frequency
Low frequency
104c
104b
104a
Oscillation frequency (MHz)
2200
2000
1800
1600
1400
1200
1000
0
1
2
3
Control voltage Vt (V)

FIG. 22


- - - - - : 104c VCO circuit
- . — . — : 104b VCO circuit
. — . . — : 104a VCO circuit
Phase noise (dBc/Hz)
-40
-60
-80
-100
-120
-140
104c
104b
104a
1
10
100
1000
10000
Offset frequency (KHz)

REFERENCE NUMERALS IN THE DRAWINGS

1 High frequency signal processing means
2a High frequency signal input terminal
2b High frequency signal output terminal
3 LO signal selecting means
4 VCO circuit group
4a, 4b, 4c VCO circuit
5, 9 Current source circuit group
5a, 5b, 5c Current source circuit
6: PLL
7 Loop filter
8 Frequency control voltage terminal
9a, 9b, 9c Variable current source circuit
11 Digital demodulation circuit
12 BER judging circuit
13 Current control means
14 Tuning means
15 Received characteristics judging means
16 Digital modulation system detection circuit
17 Digital modulation system judging circuit
18 Digital modulation system judging means
20a, 20b, 20c MIX circuit
21 High frequency input signal selecting means
22 High frequency output signal selecting means
23 Low phase noise amplifier group (LNA group)
23a, 23b, 23c Low phase noise amplifier (LNA)
24: BFP